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S3	709	$3selected adj wordline with negative or $3selected adj word adj line with negative	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:03
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S5	1175785	S4 and negative and voltage or potential	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:04
S6	161	S4 and negative and (voltage or potential)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:05
S7	97	S6 and decoder with negative with $3selected	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:05
S8	73	S7 and positive with selected with S1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:06

S9	68	S8 and "365"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:16
S10	2	"6058060".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:17

US-PAT-NO: 5

DOCUMENT-IDENTIF

TITLE: Nonv

--------- KWIC ---------

Abstract Text - ABTX (1):

There is provided a nonvolatile semiconductor memory which can simplify a circuit structure of a row decoder circuit to minimize an increase in chip size, and selectively supply a negative voltage to a word line. The nonvolatile semiconductor memory has a row decoder circuit section for selecting one of word lines in a memory cell array in response to an input address, and outputting a negative voltage or high voltage to the selected word line in accordance with a selected mode while outputting a ground potential to non-selected word lines. In such a nonvolatile semiconductor memory, each of predecoders comprises supply voltage-high voltage and ground-negative voltage converting circuits for converting the output levels into levels of supply voltage-high voltage and ground-negative voltage respectively in response to the input address, high-voltage and negative-voltage drivers for outputting from the first and second terminals the high voltage or the negative voltage in accordance with each output from these converting circuits, and a select address driver for outputting a voltage activated by the outputs of the voltage drivers and switched by the selected mode.

Brief Summary Text - BSTX (3):

The present invention relates to a nonvolatile semiconductor memory, and in particular, to a negative-voltage row-decoder circuit in a flash EEPROM (Electrically Erasable/Programmable Read Only Memory).

Brief Summary Text - BSTX (5):

When writing or erasing data into or from a flash EEPROM with memory cells each having a floating gate, application of a negative voltage to a gate of a memory transistor is a very important technique in attaining low voltage and high reliability of the device. If the writing or erasing of data is done in a small unit of capacity, a row decoder circuit to supply only a selected word line with a negative or high voltage is required.

Brief Summary Text - BSTX (6):

Now, description is made as to memory cells in such a flash EEPROM. Table 1 shows exemplary conditions of bias voltage applied to respective terminals of a memory cell when erase and write operations are performed by using Fowler-Nordheim tunnel current. FIGS. 1A and 1B are schematic sectional views of the memory cell in the respective operations. In read-out operation, a control gate 31 is supplied with 5.0 V, a drain 33 with 1.0 V and a source 32

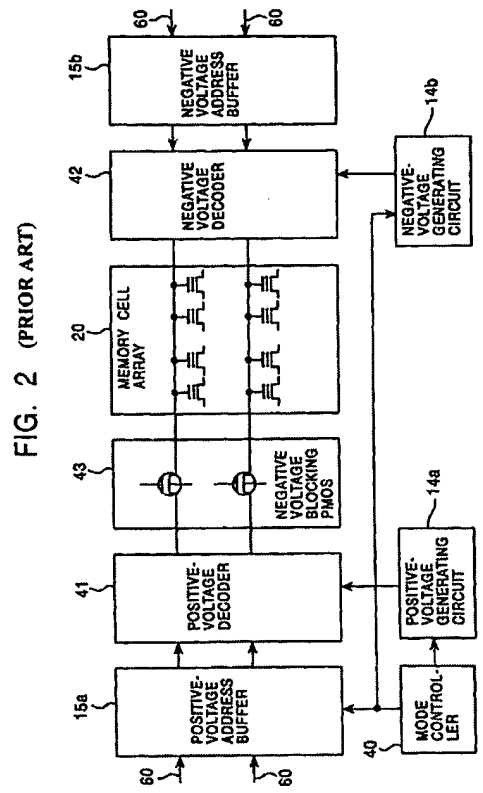

FIG. 2 (PRIOR ART)

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@PJL SET JOBATTR="JobAcct1=TLe3"
@PJL SET JOBATTR="JobAcct2=WS08

US-PAT-NO: 6

DOCUMENT-IDENTIF

TITLE: Dyna charge r

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--------- KWIC --------

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Level converter converts a word line group specifying signal, which is sent from a row decoder and has amplitude of a power supply potential Vcc and a ground potential GND, into mutually complementary logic signals WD and ZWD of a high voltage Vpp and a negative potential Vbb. An RX decoder decodes an address signal to output a signal of an amplitude of (Vpp-Vbb) specifying a word line in a word line group. A word driver provided corresponding to each word line transmits a word line specifying signal or a negative potential to the corresponding word line in accordance with signals WD and ZWD sent from a level converting circuit. The nonselected word line receives negative potential Vbb from a word driver. The selected word line receives high voltage Vpp from the word driver. It is possible to suppress a channel leak current at a memory transistor in the nonselected memory cell, which may be caused by the potential change of the word line and/or bit line, and a charge holding characteristic of the memory cell can be improved.

Brief Summary Text - BSTX (5):

FIG. 63 schematically shows a whole structure of a dynamic semiconductor memory device (will be referred to as "DRAM") in the prior art. In FIG. 63, the DRAM includes a memory cell array 900 having memory cells MC arranged in a matrix of rows and columns. In memory cell array 900, a word line WL is provided corresponding to each row of memory cells MC, and a column line (bit line pair BL and /BL) is provided corresponding to each column of memory cells MC. FIG. 63 representatively shows one word line WL and one bit line pair BL and /BL. Memory cell MC is provided corresponding to a crossing of bit line pair BL and /BL and word line WL. In FIG. 63, memory cell MC is provided corresponding to the crossing of bit line BL and word line WL, as an example. Memory cell MC includes a capacitor MQ storing information in the form of electric charges, and a memory transistor MT which is responsive to a signal potential on word line WL to be turned on to connect memory capacitor MQ to bit line BL (or /BL).

Brief Summary Text - BSTX (6):

The DRAM further includes an address buffer 902 which produces an internal address signal from an externally applied address signal, a row decode circuit 904 which decodes the internal row address signal sent from address buffer 902 to produce a decode signal specifying a corresponding word line in memory cell

Details | Text | Image | HTML | KWIC

United States Patent [19]
Tomishima et al.

[11] Patent Number: 6,097,665
[45] Date of Patent: Aug. 1, 2000

[54] DYNAMIC SEMICONDUCTOR MEMORY DEVICE HAVING EXCELLENT CHARGE RETENTION CHARACTERISTICS

[75] Inventors: Shigeki Tomishima, Kanagawa-ken Artmoto, both of Hyogo, Japan

[73] Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan

[21] Appl. No.: 09/181,562
[22] Filed: Oct. 29, 1998

Related U.S. Application Data

[62] Division of application No. 08/780,230, Jan. 28, 1997, Pat. No. 5,870,344, which is a division of application No. 08/438,780, May 10, 1995, Pat. No. 5,611,569.

[30] Foreign Application Priority Data

May 11, 1994 [JP] Japan 6-097511

[51] Int. Cl.[7] G11C 8/00
[52] U.S. Cl. 365/230.06; 365/230.03
[58] Field of Search 365/230.06, 189.11, 365/149, 218, 230.03

[56] References Cited

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5,297,094 3/1994 Nakashima 365/230.06
5,392,253 2/1995 Aimoto et al. 365/230.06
5,537,362 7/1996 Gill et al. .

FOREIGN PATENT DOCUMENTS

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4-278285 10/1992 Japan .
4-302986 10/1992 Japan .

OTHER PUBLICATIONS

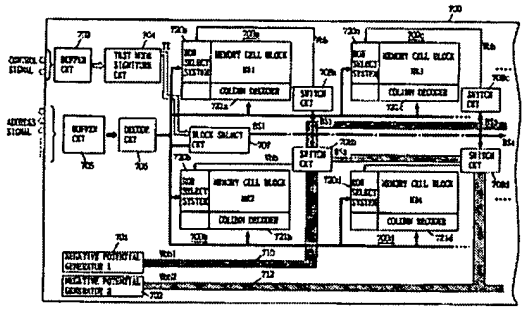
Y. Nakagome et al., "Sub-1-V Swing Bus Architecture for Future Low-Power ULSIs", 1992 Symposium on VLSI Circuits Digest of Technical Papers, pp. 82-83.

Primary Examiner—A. Zarabian
Attorney, Agent, or Firm—McDermott, Will & Emery

[57] ABSTRACT

Level converter converts a word line group specifying signal, which is sent from a row decoder and has amplitude of a power supply potential Vcc and a ground potential GND, into mutually complementary logic signals WD and ZWD of a high voltage Vpp and a negative potential Vbb. An RX decoder decodes an address signal to output a signal of an amplitude of (Vpp−Vbb) specifying a word line in a word line group. A word driver provided corresponding to each word line transmits a word line specifying signal or a negative potential to the corresponding word line in accordance with signals WD and ZWD sent from a level converting circuit. The nonselected word line receives negative potential Vbb from a word driver. The selected word line receives high voltage Vpp from the word driver. It is possible to suppress a channel leak current at a memory transistor in the nonselected memory cell, which may be caused by the potential change of the word line and/or bit line, and a charge holding characteristic of the memory cell can be improved.

21 Claims, 43 Drawing Sheets



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US-PAT-NO: 6

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TITLE: Dyna charge re

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--------- KWIC ---------

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Details | Text | Image | HTML | KWIC

US006377508B1

(12) **United States Patent**
Tomishima et al.

(10) Patent No.: US 6,377,508 B1
(45) Date of Patent: *Apr. 23, 2002

(54) **DYNAMIC SEMICONDUCTOR MEMORY DEVICE HAVING EXCELLENT CHARGE RETENTION CHARACTERISTICS**

(75) Inventors: Shigeki Tomishima; Kazutami Arimoto, both of Hyogo (JP)

(73) Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo (JP)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/467,916

(22) Filed: Dec. 21, 1999

Related U.S. Application Data

(60) Continuation of application No. 09/181,562, filed on Oct. 29, 1998, which is a division of application No. 08/789,240, filed on Jan. 28, 1997, now Pat. No. 5,870,348, which is a division of application No. 08/438,240, filed on May 10, 1995, now Pat. No. 5,617,366.

(30) Foreign Application Priority Data

May 11, 1994 (JP) 6-097211

(51) Int. Cl.[7] G11C 8/00

(52) U.S. Cl. 365/230.06; 365/189.11

(58) Field of Search 365/230.06, 189.11, 365/149, 218

(56) References Cited

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Primary Examiner—A. Zarabian
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

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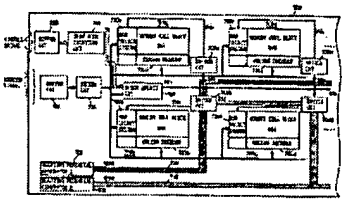
45 Claims, 43 Drawing Sheets



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Details | Text | Image | HTML | KWIC

US005870348A

United States Patent [19]
Tomishima et al.

[11] Patent Number: 5,870,348
[45] Date of Patent: Feb. 9, 1999

[54] DYNAMIC SEMICONDUCTOR MEMORY DEVICE HAVING EXCELLENT CHARGE RETENTION CHARACTERISTICS

[75] Inventors: Shigeki Tomishima; Kazutami Arimoto, both of Hyogo, Japan

[73] Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan

[21] Appl. No.: 789,240

[22] Filed: Jan. 28, 1997

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[62] Division of Ser. No. 436,790, May 10, 1995, Pat. No. 5,617,360.

[30] Foreign Application Priority Data

May 11, 1994 [JP] Japan 6-097511

[51] Int. Cl.[6] G11C 8/00

[52] U.S. Cl. 365/230.06; 365/189.11; 365/149

[58] Field of Search 365/230.06, 149, 365/189.11, 189.09, 218

[56] References Cited

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Primary Examiner—A. Zarabian
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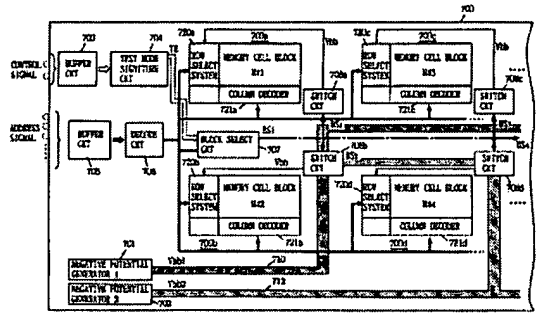
12 Claims, 43 Drawing Sheets



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